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Docket No.: 057810-0032

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Masayuki HATA, et al.	:	Confirmation Number: 2755
Application No.: 10/081,180	:	Group Art Unit: 1722
	:	Allowed: April 27, 2005
Filed: February 25, 2002	:	Examiner: Robert M. Kunemund

For: NITRIDE-BASED SEMICONDUCTOR ELEMENT AND METHOD OF FORMING NITRIDE-BASED SEMICONDUCTOR

COMMENTS RESPONSIVE TO STATEMENT OF REASONS FOR ALLOWANCE UNDER 37 C.F.R. § 104(e)

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Statement of Reasons for Allowance accompanied the April 27, 2005 Notice of Allowability regarding the above-identified application. Entry of that Statement into the record should not be construed as any agreement with or acquiescence by Applicants in the stated reasoning.

On page 2 of the Notice of Allowability, the Examiner offered a statement of reasons for allowance. However, the Examiner's reasons contain a clearly inaccurate interpretation of the claimed invention. Specifically, the Examiner offered the following statement:

> This is followed by a two step growth of semiconductor nitrides.

This statement is not accurate, because the first nitride based semiconductor layer is not formed by a two-step growth process. Rather, the first nitride based semiconductor layer is formed by a single step growth process. This should be apparent from the written

description of the specification, notably commencing at page 19, line 15 through page 20, line 11, and with respect to Figs. 4 through 6.

Indeed, adverting to Figs. 4 through 6 and the above cited portion of the written description of the specification, it should be apparent, and one having ordinary skill in the art have understood that the first nitride based semiconductor layer is grown by a single step process, but growth proceeds in different directions during different stages because of the topographical profile on the substrate, as shown in Fig. 3, noting buffer layers 3 and mask 2. Thus, when the single step growth process of the first nitride base semiconductor layer is implemented, initial growth occurs on buffer layers 3 (paragraph bridging pages 19 and 20 of the written description of the specification), then laterally on mask 2 (Fig. 5; first full paragraph on page 20 of the written description), followed by coalescence to form the single first nitride base semiconductor layer 4 illustrated in Fig. 6 (page 20 of the written description, lines 8 through 12). As should be apparent from the second full paragraph on page 20 of the written description of the specification, growth of the first nitride based semiconductor layer occurs in a single step, but proceeds during stages in different directions only because of the topographic profile of the substrate on which is it grown.

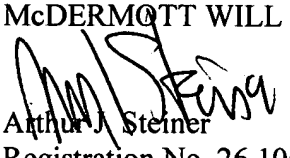
Applicants comments on the Examiner's reasons for allowance are offered to clarify the record in that the first nitride based semiconductor is formed in one step, not two steps as asserted by the Examiner. It is respectfully submitted that the allowed claims should be entitled to be the broadest reasonable interpretation and broadest range of equivalents in light of the language of the claims, the supporting disclosure and Applicants' prosecution of the claims, without reference to the Examiner's statement of reasons for allowance.

To the extent necessary, if any, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the

filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Arthur J. Steiner
Registration No. 26,106

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 AJS:MWE
Facsimile: 202.756.8087
Date: June 29, 2005

Please recognize our Customer No. 20277 as our correspondence address.